

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Masao SHINOZAKI et al.

Appln. No.:

Filed: Herewith

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING A
SEMICONDUCTOR DEVICE

* * *

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified
patent application as indicated below.

IN THE CLAIMS:

Please amend Claims 3, 4 and 7 as set forth below.

- 1 3. (Amended) A semiconductor device according to Claim
- 2 1, wherein a power supply voltage applied to the first MOS
- 3 transistors constituting the input circuit or the output

4 circuit is equal to a power supply voltage applied to the
5 second MOS transistors constituting the internal circuit.

1 4. (Amended) A semiconductor device according to Claim
2 2, wherein a gate length of the first MOS transistors is equal
3 to a gate length of the second MOS transistors.

1 7. (Amended) A semiconductor device according to Claim
2 1, wherein a power supply voltage applied to the first MOS
3 transistors constituting the input circuit or the output
4 circuit is higher than a power supply voltage applied to the
5 second MOS transistors constituting the internal circuit.

Please add the following claims:

1 21. (New) A semiconductor device according to Claim 2,
2 wherein a power supply voltage applied to the first MOS
3 transistors constituting the input circuit or the output
4 circuit is equal to a power supply voltage applied to the
5 second MOS transistors constituting the internal circuit.

1 22. (New) A semiconductor device according to Claim 21,
2 wherein a gate length of the first MOS transistors is equal to
3 a gate length of the second MOS transistors.

1 23. (New) A semiconductor device according to Claim 3,
2 wherein a gate length of the first MOS transistors is equal to
3 a gate length of the second MOS transistors.

1 24. (New) A semiconductor device according to Claim 21,
2 wherein a gate insulating film thickness of the first MOS
3 transistors is equal to a gate insulating film thickness of
4 the second MOS transistors.

1 25. (New) A semiconductor device according to Claim 21,
2 wherein an area of the active region in which the first MOS
3 transistors are formed is larger than an area of the active
4 region in which the second MOS transistors are formed.

1 26. (New) A semiconductor device according to Claim 2,
2 wherein a power supply voltage applied to the first MOS
3 transistors constituting the input circuit or the output
4 circuit is higher than a power supply voltage applied to the
5 second MOS transistors constituting the internal circuit.

REMARKS

Claims 3, 4 and 7 have been amended to avoid the multiple dependent claim surcharge. Claims 21-26 presented herein correspond to the dependencies eliminated from the amended claims.

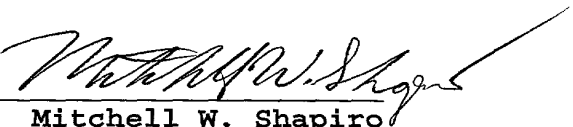
The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees that may be required by this paper and to credit any overpayment to that Account.

Respectfully submitted,

MWS:jab

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By:


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Reg. No. 31,568

December 5, 2001

MARKED-UP VERSION OF THE CLAIMS:

1 3. (Amended) A semiconductor device according to Claim 1
2 [or Claim 2], wherein a power supply voltage applied to the
3 first MOS transistors constituting the input circuit or the
4 output circuit is equal to a power supply voltage applied to
5 the second MOS transistors constituting the internal circuit.

1 4. (Amended) A semiconductor device according to Claim 2
2 [or Claim 3], wherein a gate length of the first MOS
3 transistors is equal to a gate length of the second MOS
4 transistors.

1 7. (Amended) A semiconductor device according to Claim 1
2 [or Claim 2], wherein a power supply voltage applied to the
3 first MOS transistors constituting the input circuit or the
4 output circuit is higher than a power supply voltage applied
5 to the second MOS transistors constituting the internal
6 circuit.